Improvements Within APT

—— *Chapter 4* ——

This chapter is designed to provide the student with general knowledge about the main improvements regarding the APT part of AXE 810. It describes the new hardware as well as main changes and improvements within APT hardware.

OBJECTIVES:

Upon completion of this chapter the student will be able to:

- describe the main building-blocks of the new hardware used in AXE 810

- describe the main improvements regarding the group switch hardware

- describe the main improvements regarding echo cancellers, ET devices, and transcoders located in the GEM subrack

- describe main changes of hardware located in the GDM subrack

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4 Improvements Within APT

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THE GEM SUBRACK

The GEM subrack is one of the two cornerstones in the new APT hardware. GEM, which stands for Generic Ericsson Magazine, is the main building block in APT and it can hold many important and fundamental APT functions:

- Group Switch

- ET155

- Transceivers

- Echo Canceller

- Interfaces to GDM subracks

This means that the majority of hardware devices will be located in the GEM subracks. Hardware not included in GEM is located in the GDM, Generic Device Magazine. More about GDM later on in this chapter.

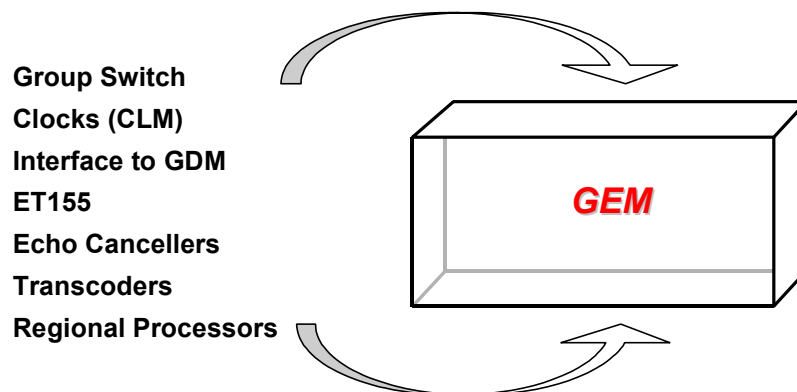The main principle of GEM can be seen in the figure below.

Group Switch
Clocks (CLM)
Interface to GDM
ET155
Echo Cancellers
Transcoders
Regional Processors

GEM

Figure 4- 1 GEM is the basic building block in AXE 810

THE SUBRACK AND INTERFACES

Each GEM subrack is a generic piece of hardware which holds some mandatory boards but has 22 generic positions which can be used to house any type of board which is adapted to the GEM size and backplane. This creates a flexible solutions with many alternatives. The mandatory boards are:

- Two maintenance processors which take care of maintenance functions inside the subrack. The board is referred to as SCB-RP, Support and Connection Board with RP.

- Two group switch boards with a capacity of 16K ports of 64 kbit/s.

Beside these 4 boards, there are 22 positions that are free for usage. The figure below shows the main principle.
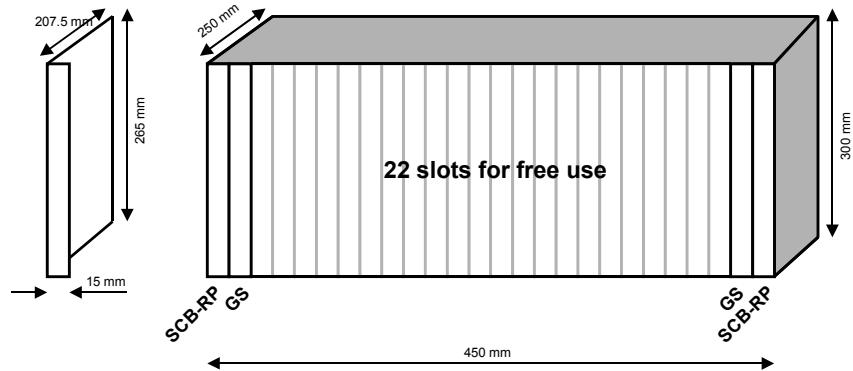

Figure 4- 2 The mandatory and free slots in GEM

The connection of devices to the group switch is done via the backplane. The interface is a new type of group switch interface with the name "DL34". This interface is a flexible interface with a capacity of 128-2096 time slots of 64 kbit/s. The bit rate is 222.2 Mbit/s. This means that an ET155 board, which terminates up to 63 x 2.048 Mbit/s = 2016 time slots, can be connected via the DL34 interface. Devices with lower bit rate can of course also be connected as the number of channels is flexible. The figure below shows the main principle.
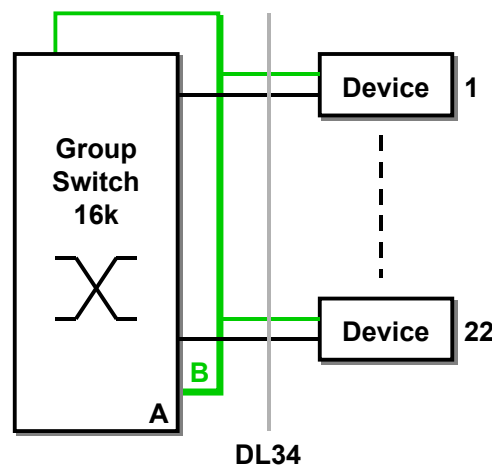

Figure 4- 3 Interfaces to the group switch inside the GEM subrack

The processing power for the device boards is supplied by the on-board integrated RPs that was mentioned in chapter 3. In the backplane of the GEM subrack, there are several busses. From a

control point-of-view, the following two are the most interesting:

- a duplicated RP bus (serial RP bus)

- a 100 Mbit/s Ethernet for future use.

The figure below shows the control structure inside the subrack as well as the Ethernet connection which can be used by future applications. The boxes inside the boards represents the new regional processors which are integrated on the board, the RPI.
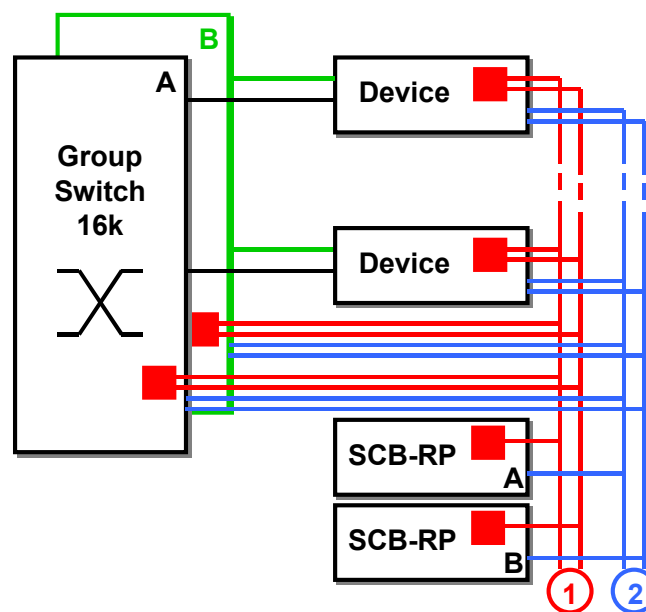

Figure 4- 4 The control structure inside GEM

The bus with number 1 is a duplicated serial RP bus in the backplane of the GEM subrack. The RP bus terminates in the RP Handler subrack of the Central Processor. The bus with number 2 in the figure is the duplicated 100 Mbit/s Ethernet bus which will be used by future applications. The SCB-RP has an Ethernet switch as well as one 1Gbit/s and one 100 Mbit/s Ethernet interface to the front of the board. It will be used by future functions in AXE.

CONNECTION OF GDM

AXE equipment inside the older GDM subracks (GDM stands for Generic Device Magazine) must in some way be able to co-exist with the new GEM subracks. This is achieved by means of duplicated interface boards called DLEB inside the GEM subrack. These boards interface the DL3 interface from the GDM subrack. The DL3 interface is a 48Mbit/s (34 Mbit/s) interface which was used as the main interface to the old 128K

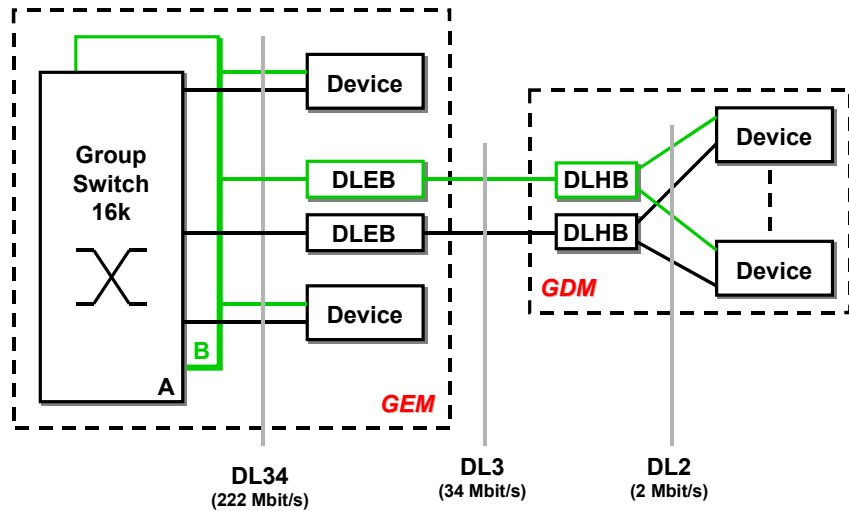group switch in APT HWM 1.3 and 1.4. The figure below shows the main principles.

Figure 4- 5 Connection of GDM subracks to GEM

DLEB stands for "Digital Link multiplexer for Existing equipment Board" and DLHB stands for Digital Link Handling Board. Each DLEB board can connect up to 4 DLHB boards (up to 4 GDM subracks) and there is always a need for two DLEB board; one for each plane in the group switch.

RESTRICTIONS

One important restriction when it comes to configuring the GEM subrack is that all positions in the subrack cannot house ET155 boards. The main reason is that 22 ET155 exceeds the switch capacity in the subrack which is 16k. One ET155 takes up to 2k so there can be up to 8 ET155 in the same subrack. A need for more ET155 boards is just spread out among several GEM subracks. Please note that these figures assumes fully used ET155. More ET155 may be located in the GEM subrack if not fully used.

THE NEW GROUP SWITCH

GENERAL

The new group switch in AXE 810, which is referred to as GS890, is a completely new switch. In earlier AXE modernisations, the group switch structure has been the same but the hardware has been modified and extended to 128K. This time, the group switch is new. The main features are:

- Distributed architecture
  The switch is located in every GEM subrack as indicated earlier in this book.

- Time-Space architecture
  The old AXE group switch had a time-space-time (TST) architecture. This new one has a time-space (TS) architecture creating better characteristics.

- Maximum size of 512K
  The switch can be scaled up to 512K multiple positions (64 kbit/s channels). This means that the switch can have more than 250 000 calls established at the same time (theoretically).

- Subrate switch up to 128K
  The size of the subrate switch can be extended up to 128K. The subrate is used in mobile applications. The implementation of the subrate switch differs from earlier GS hardware.

- Strictly non-blocking
  The old group switch in AXE was not strictly non-blocking as each inlet could be loaded to about 80%. The new architecture with time-space structure gives this advantage.

- Reduced cabling
  The cabling has been reduced to about 1/12 if compared with the old switch (GS12).

- Reduced power consumption
  The power consumption has been reduced to 1/6 of the old switch's power consumption for the same switch size (GS12).

- Reduced space
  The floor space is reduced significantly as a 16K subrack now is one circuit board. If compared with the old BYB 202 based switch, the changes are enormous as one 16K switch needed 32 TSM magazines occupying several cabinets.

- Device protection without waste of multiple positions
For ET155, protection switching is an option. In that case, the interface to the group switch can connect two ET155:s without wasting multiple positions.

The architecture of the switch is further described in the following chapters.

HARDWARE

The main hardware when it comes to switching is the XDB board (X means switching and DB stands for "distributed board"). The XDB boards has a switching capacity of 16K and there are two in each GEM subrack, one for the A-plane and one for the B-plane.
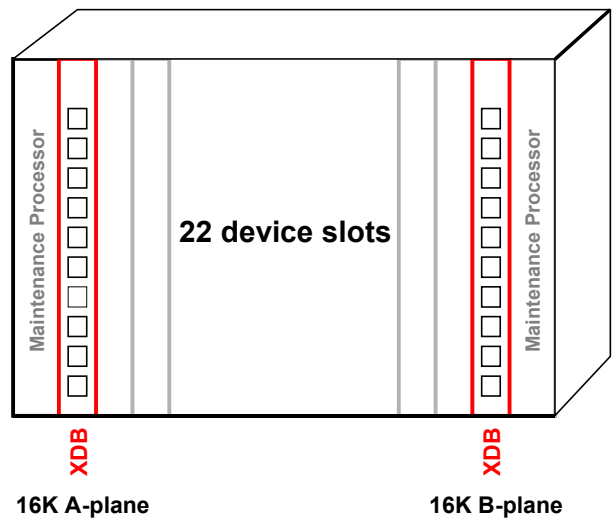

Figure 4- 6 The XDB boards in GEM

On the XDB board, there are three ASICs (application specific integrated circuit) which implements the 16K switch. One ASIC is a multiplexer and two are holding the speech stores (SS) and control stores (CS). One integrated Regional Processor (RPI) is also on the XDB board. The devices in the subrack are connected to the XDB boards via the backplane while connection to other XDB boards are done via cables connected at the front of the board. The figure below shows the XDB board.
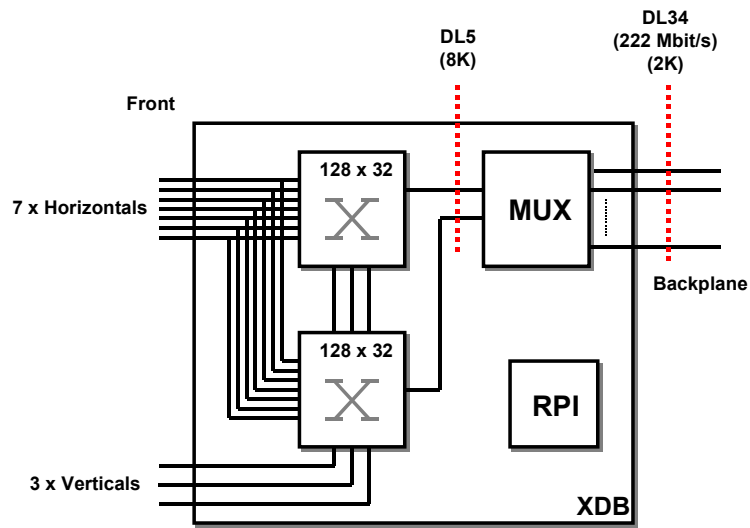
Figure 4- 7 Circuits on the XDB board

The structure of the switch is explained in next chapter.

STRUCTURE

If you only have a 16K group switch, it is enough to have just one XDB circuit board. However, in case of larger switches, the XDB boards have to be inter-connected by means of so-called horizontal and vertical connections. The horizontal and vertical connections are best explained if you imagine all XDB boards put in a matrix. The figure below shows the main idea.
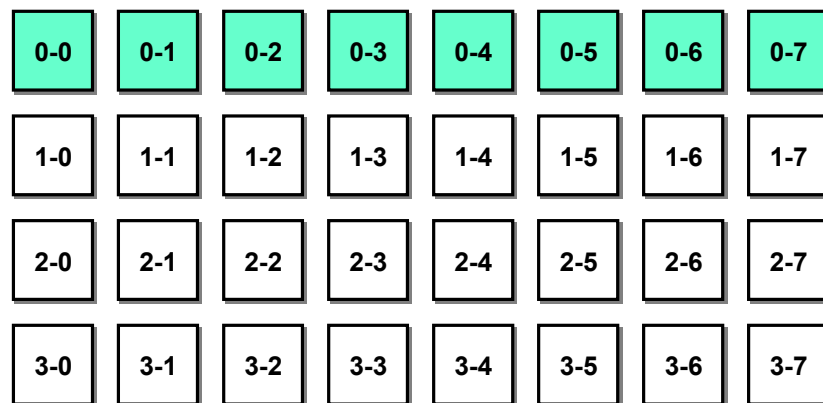

Figure 4- 8 A matrix of switch boards.

Each board has a capacity of 16K so the maximum capacity in the switch is 4 rows x 8 columns x 16K = 32 x 16 = 512K.

Horizontals and Verticals

The inter-connection of the boards in the switch is done by two different types of connections:

- Horizontals
  These connections connect all switch boards in a row to each other. The connection is "all to all" meaning that all boards in a row have direct connections to all other boards in the same row.

- Verticals
  These connections connect all switch boards in a column to each other. Also these connections are "all to all".

Showing all cables from all switch boards in a 512K switch is difficult but the figure shows all the cabling going to and from the first board (0-0) in the switch matrix.
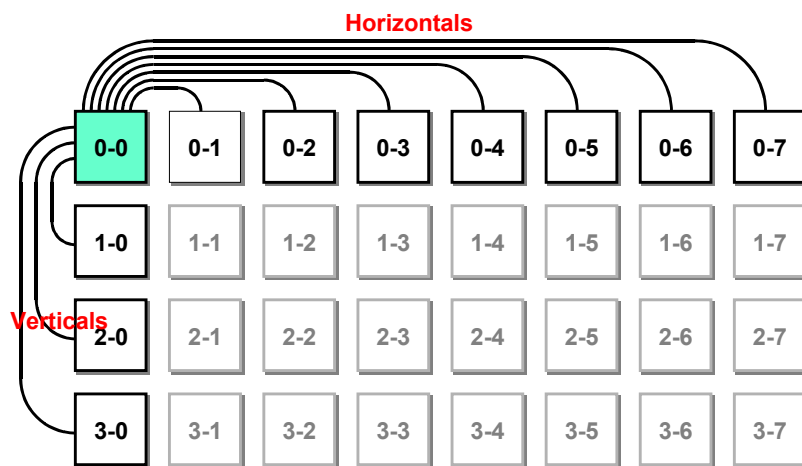

Figure 4- 9 Cabling from one switch board (note that all cables are not shown in the figure)

The Switching

In order to understand how switching is made, the figure must be simplified even more. As all switch boards within the same row are inter-connected by horizontals, and all switch boards within the same column are inter-connected by verticals, the figure could be drawn like the one below.
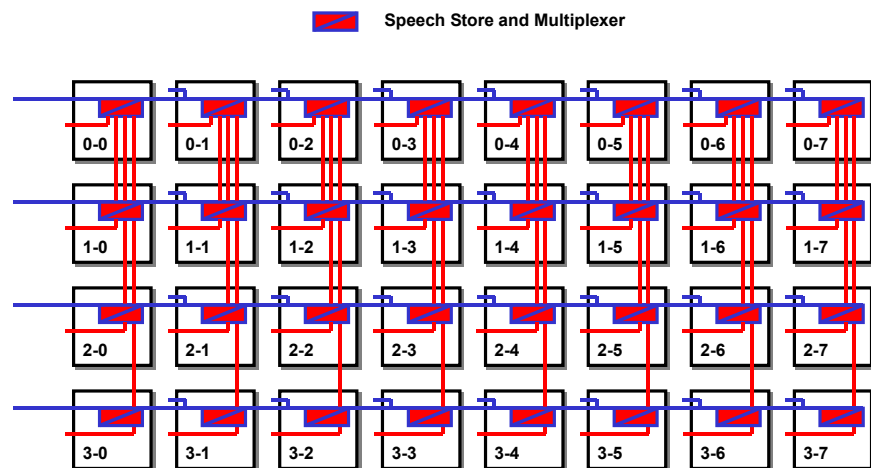
Figure 4- 10 A switch matrix with horizontals and verticals
(simplified, as verticals are only shown from row 0)

The principle of switching is as follows:

1. A speech sample comes in on a horizontal and is then copied
    to all speech stores on that row. The horizontals takes care of
    that.

2. The time switching takes place in the speech store of the
    correct column and the speech sample is sent on the vertical
    to the correct board.

3. On the destination board, a multiplexer takes the correct
    speech sample from the vertical.

The switching in the other direction works according to the
same principle but that will take another path. The figure below
shows the main principle of switching between two switch
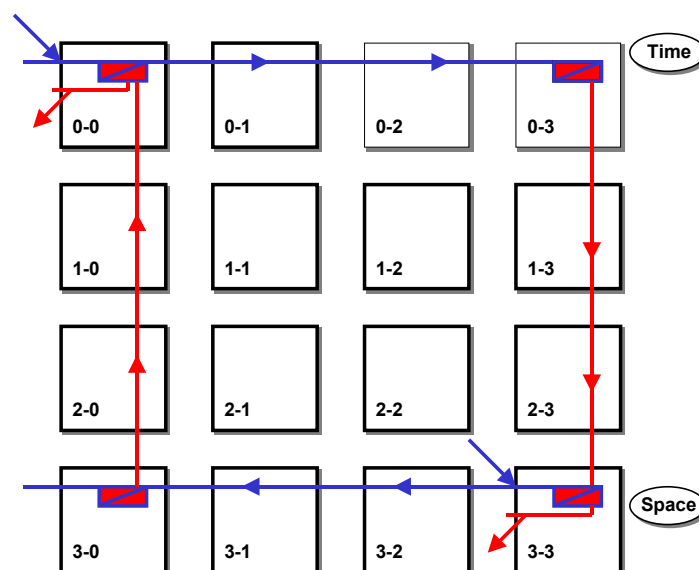boards in a part of the switch.

Figure 4- 11 Switching in both directions.

It can be seen that the samples take different paths. The rule is always to copy the speech sample to all speech stores on the same horizontal (in the same row) and then switch to the correct vertical.

Subrate

Subrate is used in mobile applications (for example in the BSC in GSM) to allow one 64 kbit/s channel to include more than one call. For example, most mobile systems code speech to less than 8 kbit/s which means that one 64 kbit/s channel can send 8 calls. To be able to switch these sub-rate channels, the group switch must be designed in a special way.

In the "old" group switches, the subrate switch was a "back pack" solution with a special subrack implementing the switch. The maximum capacity was 4K in all earlier version of AXE. The figure below shows the main principle of the old subrate solution.
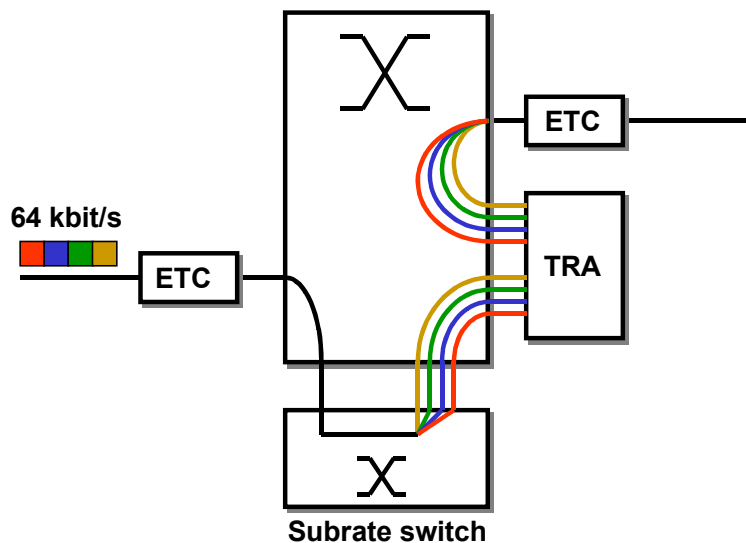

Figure 4- 12 Subrate in the old group switch

The subrate solution in the new GS890 is implemented in the first row of the switch. This row has the capacity of 128K and the same hardware can be used for both subrate and normal rate. However, if the subrate function is used, the maximum size of the switch is limited to 128K. This size should be enough for any type of BSC implementation. The figure below shows the part of the switching matrix where subrate can be used.
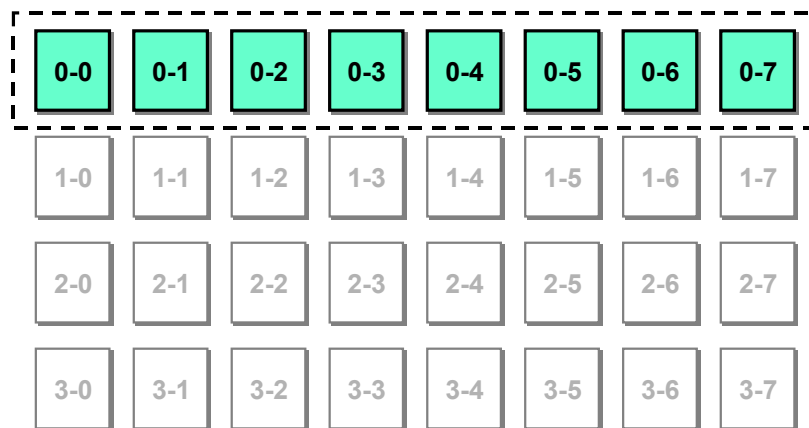
0-0	0-1	0-2	0-3	0-4	0-5	0-6	0-7
1-0	1-1	1-2	1-3	1-4	1-5	1-6	1-7
2-0	2-1	2-2	2-3	2-4	2-5	2-6	2-7
3-0	3-1	3-2	3-3	3-4	3-5	3-6	3-7

Figure 4- 13 Subrate can only be used in the first row of the group switch.

Wideband

Wideband means that the group switch hardware can be used to set-up several 64 kbit/s channels that are kept together. For example, an ISDN subscriber using both B channels for internet access, must have 2 x 64 kbit/s switched though the exchange. The new GS890 can handle wideband in the same way as previous switches; it can establish up to 31 x 64 kbit/s through the switching hardware with the order kept of the channels.

Modularity

The switch has two main limitations when it comes to how it can be built:

- The subrate part must be in the first row. One row has the capacity of 128K which is the maximum capacity of the subrate switch.

- All rows and all columns must be of same length. This has to do with the switching principle explained in the previous chapter.

The figure below gives some example of possible switch configurations. Please note that when this book is written, no high-level packages have been created so only some examples of theoretical switch configurations are shown.
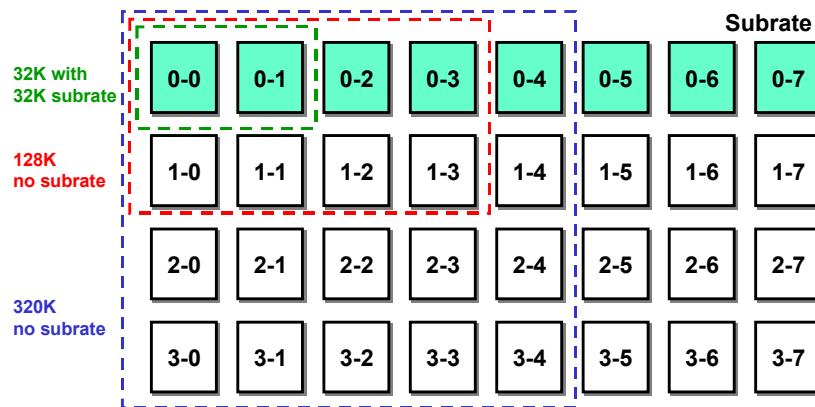
Figure 4- 14 Switch sizes, examples

Please note that the extension must create a rectangle because of the switching principle. As an example, if you have a 128K switch as in the figure above, it is not possible to just add one 16K switch (2-0 or 0-4). One column or one row must be added.

Reliability

Just as with previous group switches from Ericsson, the whole switch is duplicated. The two parts are referred to as A-plane and B-plane. Each device is connected to both planes and the system will not be disturbed for single hardware faults.

SYNCHRONISATION

A new synchronisation system is developed for the GEM subrack and the new hardware in the group switch. The exchange clock system is called CL890. The Clock Module (CLM) is now duplicated and located in the GEM subrack (or in different GEM subracks). Inside the CLM, there are two clocks for reliability. From the two CLMs, timing information is distributed to all XDB boards in both planes. This means that there are two CLMs and not three as in earlier versions. However, there are two clocks inside each CLM. Please study the figure below.
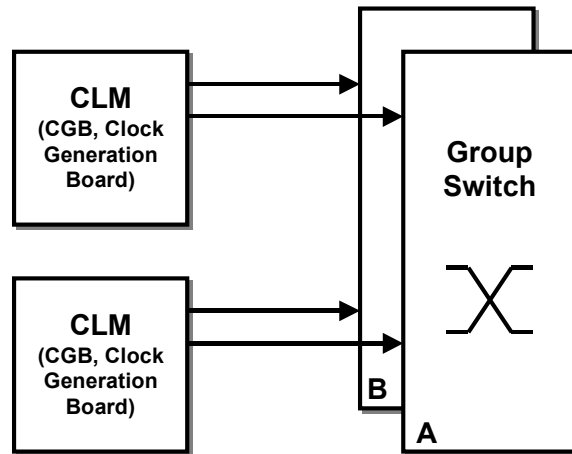
Figure 4- 15 Clock Modules provide timing information

External synchronisation of a node in a network must be possible in different ways. The exchange clock system in CL890 supports the following:

- A local reference clock in case of interrupt of external timing information. The function is referred to as Reference Clock Module (RCM) and the hardware is called Local Reference Board (LRB). This gives better long-term stability that just having the CLMs.

- External references from incoming PCM lines or external sources from other vendors. These references are connected via one or two Incoming Reference Board (IRB) which converts the incoming source to 8 kHz.

- Stand alone clocks like the Ericsson Central Building Clock (CBC) or the GPS System Clock (GSC).

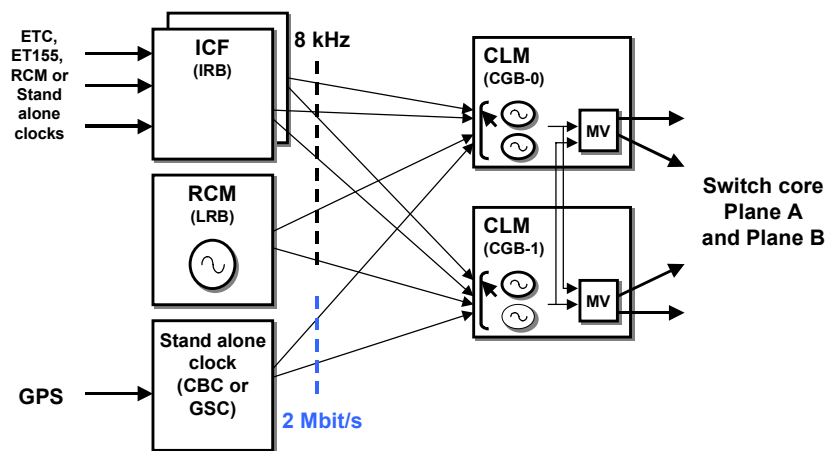The figure below gives a summary of the different alternatives.

Figure 4- 16 Clock Architecture in GS890

Depending of the planned maximum size of the group switch, different configuration alternatives exist for the clocks. The three following alternatives exist:

1. Clocks for a GS consisting of one GEM (16k)
    In this case, everything can be housed in the same GEM subrack. The subrack could lock like the example below.
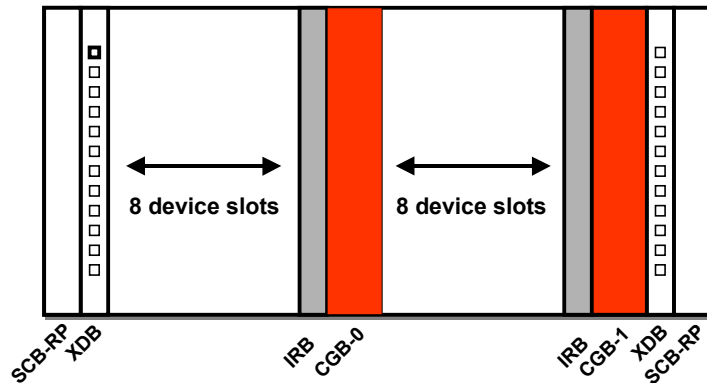

Figure 4- 17 Clocks for one GEM

2. Clocks for a GS built with 8 GEMs (128k)
    Two of the GEMs have a CGB board, one IRB board and two CDB boards for distribution of timing information. Please study the example below. All other GEMs (1-6) only have the XDB boards as the cables terminate in these boards.
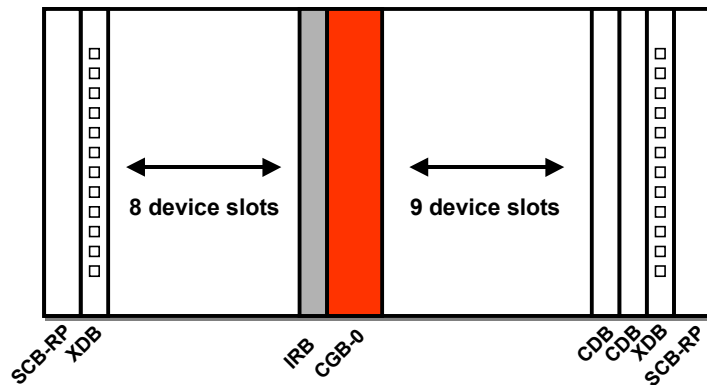

Figure 4- 18 Clocks for GS up to 128k

3. Clocks for a GS built with 32 GEMs (512k)
    With this size of group switch, there are 64 switch boards (XDB) in both planes that need timing information. It is therefore needed with two separate clock subracks Clock Distribution Magazine (CDM) which holds clocks, incoming references and distribution boards. The figure below also shows two LRBs (Reference Clock Modules) but they are optional.
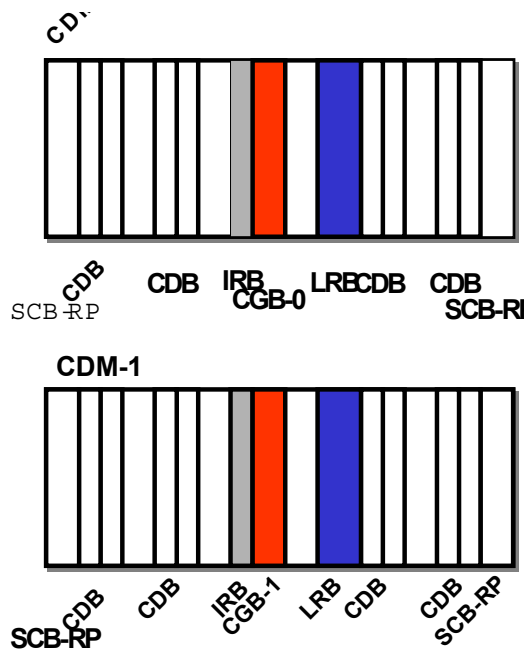
CDM-0

SCB-RP CDB   CDB   IRB CDB LRBCDB   CDB SCB-RP
                      CGB-0

CDM-1

SCB-RP CDB   CDB   IRB CGB-1 LRB CDB   CDB SCB-RP

Figure 4- 19 Clocks for GS up to 512k

CABLING

Cabling from XDB boards

It has already been mentioned that an XDB board (the switch in the GEM subrack) is connected to both horizontals and verticals. By studying the front of the board, that is quite easy to see as there are 3 vertical connections and 7 horizontal connections. The board also has 2 connectors for connection of clocks (timing information from CLMs). The figure below shows the front of the XDB board.
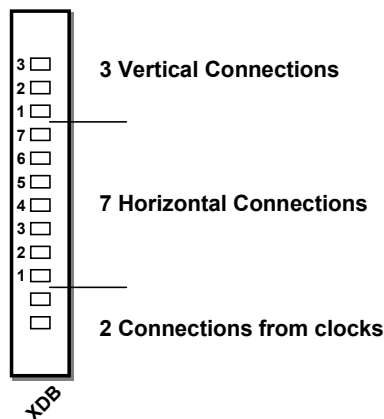

Figure 4- 20 Front of XDB board

Cabling for clocks

The cabling from the clocks to the XDB boards, and also between the two CGB boards, is slightly more complicated. The main reason is that there are many different alternatives depending on expected maximum size of the group switch (i.e. the number of GEM subracks. The example in this book will be a group switch with a size between 32K and 128K (2-8 GEM subracks). If the switch is larger than 128K, two separate subracks will be used for the clocks (as described earlier).

The example has three GEM subracks where there is only clock module in each one of the two first. In these two subracks, there are two clock distribution boards as well (CDB). The figure below shows the principle of the cabling with 3 GEM subracks.
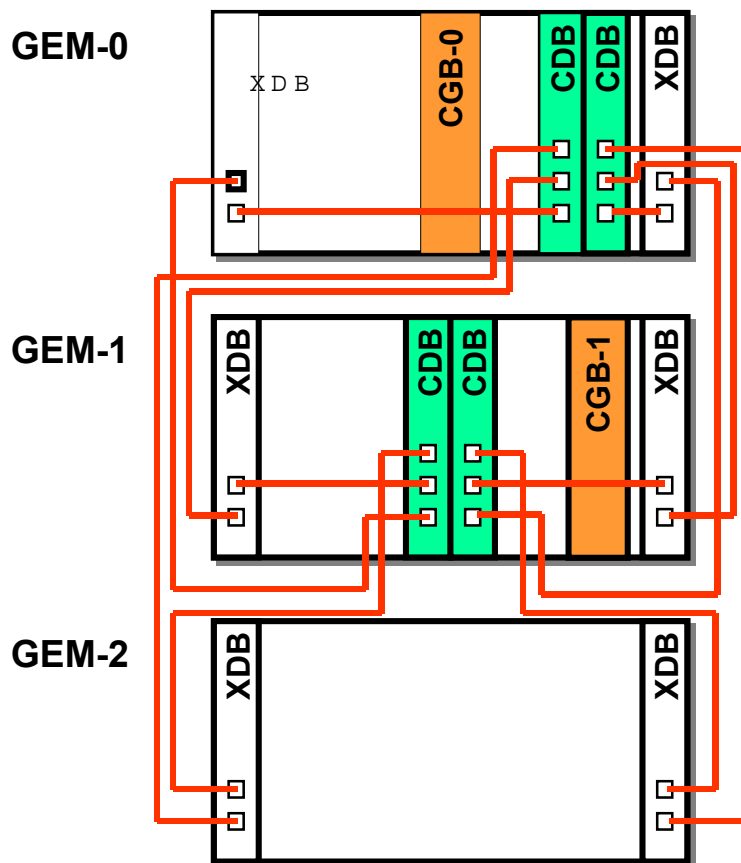

Figure 4- 21 Cabling between GEMs for clocking information

SINGLE-BOARD ET155

ET155 is not new in that sense that it existed also in APT 1.4. However, the ET155 released in AXE 810 is a single board solution which reduces footprint and power consumption considerably. The same board may be used for all three main transport standards: ITU, SONET and TTC standards (European, American and Japanese standards). By having one single board for the 155 Mbit/s interface gives a number of advantages to the customers:

- Simplified connection to the transport network due to large savings in cabling and DDF (if compared with the use of 2 Mbit/s interfaces).

- reduced footprint

- reduced power consumption

- reduced cabling

- simplified handing.

The table below makes a comparison between the versions available in AXE Classic, HWM 1.3 and HWM 1.4 and the new single board ET155. Please note that the comparison is made with the European version (E1) and that the savings in footprint and power consumption is even larger if compared with the US or Japanese versions (T1/J1).

	ETC in BYB 202 (2 Mbit/s)	ETC in BYB 501, 1.3 (2 Mbit/s)	ETC in BYB 501, 1.4 (155 Mbit/s)	Single board ET155
Footprint	~160	~ 44	4.5	1
Power Consumption	-	-	5	1
Number of boards	63 + RP + Multiplexer	63 + RP + Multiplexer	5 to 6	1
Cost for large DDF	Yes	Yes	No, but small ODF	No, but small ODF

Figure 4- 22 The new single-board ET155 compared with older versions

Another way to look at the savings in using the new ET155 is to study how they are connected to the transport network and then compare that with the connection of E1 or T1 interfaces. Please study the figure below in order to see how an AXE exchange is connected with E1 links to the transport network.
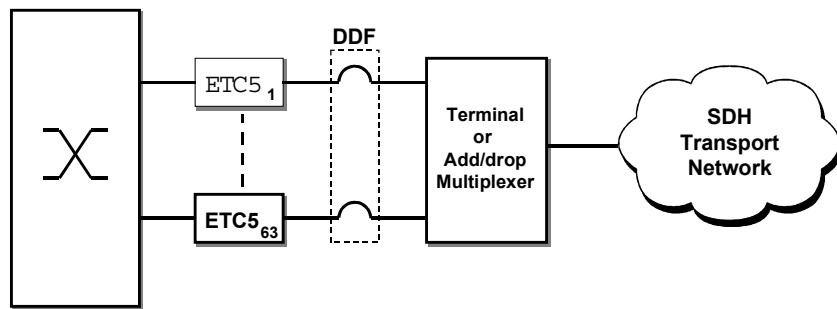
Figure 4- 23 Connection of AXE with E1 links

If the same capacity is needed but an ET155 is used instead, the picture is much simpler. The figure below shows the situation.
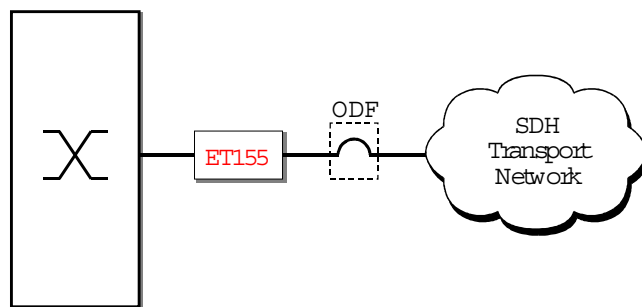

Figure 4- 24 Connection of AXE with the new ET155

The number of exchange terminals is reduced if using ET155 instead of the old ETC5 having a 2 Mbit/s interface. If upgrading from AXE HWM 1.4 to the new hardware, also there a significant saving can be achieved. Please study the figure below.
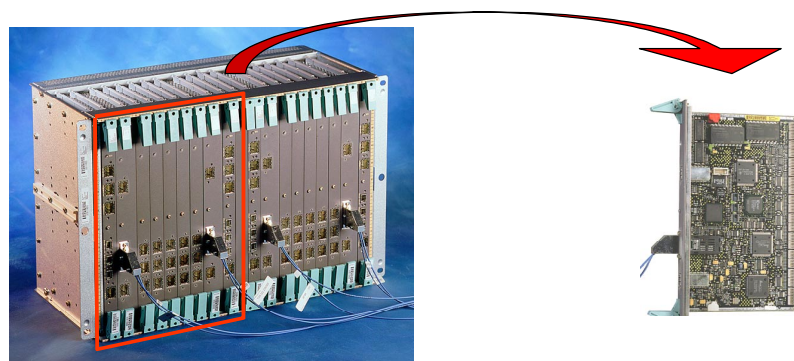

Figure 4- 25 The new ET155-1 hardware is much smaller

The protection function is important as more and more calls are sent through the same piece of hardware. In the old ET155-7, the protection was distributed on separate boards. In case of the new ET155-1, the protection is based upon the fact that there is one active ET155-1 and one stand-by. Please study the figure below.
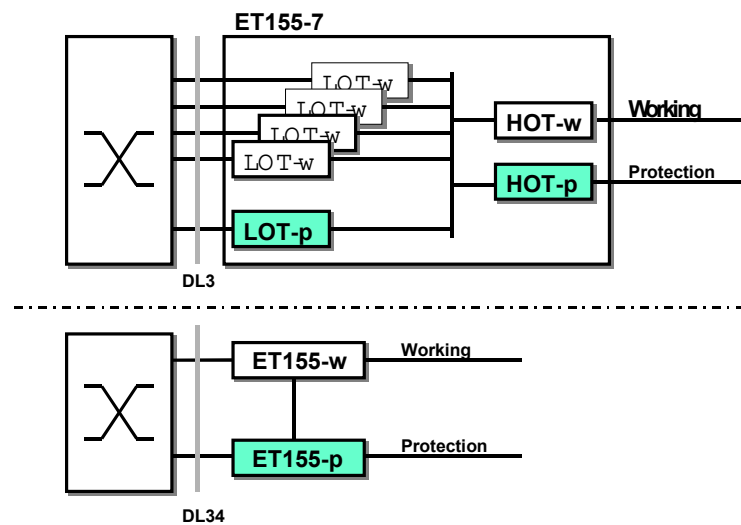
Figure 4- 26 Protection function

The list of functions in ET155 is quite long. To summarise it, please look at the list below.

- 155 Mbit/s SONET termination in accordance with ANSI standards OC3 IR-1,ANSI T1105.06-1996; 1310 nm

- 155 Mbit/s SDH termination in accordance with ETSI, ITU-T, ANSI and TTC standards

- Automatic Protection Switching (APS), option

- Hardware inventory support

- Audible tone sending and attenuation on 64 kbit/s channels

- MTBF > 25 years

- MTBF with protection (APS) > 50 000 years

TRANSCODERS, TRA

POSITION OF TRA

Transcoders are used in mobile systems to change the coding from the ordinary PCM coding with 64 kbit/s to a lower bit rate. The main reason for changing the coding is that PCM is not well suited for radio transmission due to high bit rate and no functions for handling transmission errors often occurring on the radio path. The transcoders are located in the Base Station Controller in GSM. The figure below shows the position of the transcoder in the system.
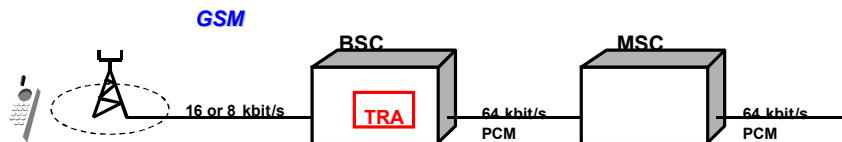

Figure 4- 27 The position of the transcoders in mobile systems

THE FUNCTION OF THE TRA

As already described is one of the main problems with mobile communication the bad radio connection. This requires a special coding format for the speech in order to reduce number of bit/s and to increase speech quality. The job of the transcoder is to convert between different coding standards. The coding standards used in the fixed part of the mobile network is always 64 kbit/s PCM. However, in the mobile interface, there are a number of standards. To give an example, we can study GSM which today has three different coding standards defined:

- Full Rate (FR)
  This was the first coding standard in GSM and it codes speech with 13 kbit/s.

- Enhanced Full Rate (EFR)
  This coding format gives better speech quality but with maintained bit rate of 13 kbit/s. The algorithm demands more processing power.

- Half Rate (HR)
  This algorithm is used to increase the capacity in the system as twice as many mobiles can be served. It gives lower speech quality and the bit rate is 6.5 kbit/s. The speech coding algorithm demands more processing power than EFR.

This means that the transcoders must be able to support a number of different speech coding algorithms at the same time. The figure below shows the main function of the transcoder.

Figure 4- 28 Main function of transcoder, TRA

The coded speech in GSM will be 6.5 kbit/s but this bit stream is put in an 8 kbit/s bit stream (1/8 PCM channel) due to the fact that the subrate works on 8 kbit/s level. Additional 1.5 kbit/s is filled with signalling and padding (rate adaptation).

THE NEW TRA HARDWARE

The new hardware for transcoders is built round a speech processing platform called CSPB, Common Speech Proccessing Board. The capacity has been increased significantly if compared with the previous versions. Please study the table below.

	TRA R5 (GSM)	TRAB3 (TDMA)	TRA R6 (GSM)
Channels per board	24	48	192
Capacity	1	1	8
Volume	1	1	1/8
Power consumption	1	1	1/3

Figure 4- 29 Capacity of the new TRA hardware

The transcoder hardware is located in the GEM subrack as indicated earlier and they are in that way connected to the Group Switch. In that way, they are connected in "pool" which means that they are connected to different base stations when needed. This gives redundancy and a possibility to connect transcoders on demand. The figure below shows the main idea.
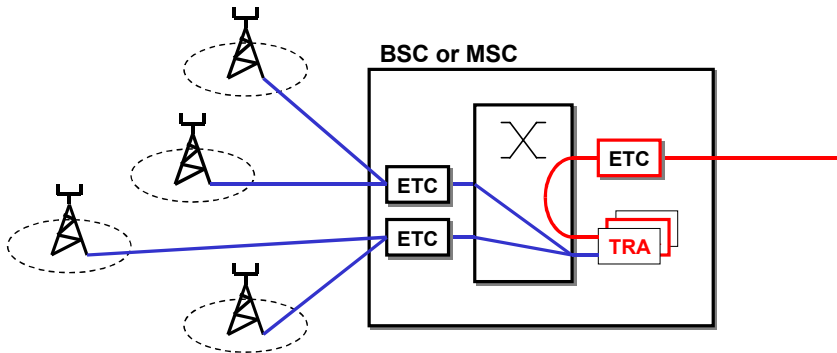
Figure 4- 30 Transcoders connected in a pool

ECHO CANCELLERS IN POOL, ECP

THE PROBLEM WITH ECHO

The echo canceller is a device which is connected to the speech path to remove echo caused by long delays in the speech path. Some speech energy leaks back in the analogue line circuit and returns to the sender. It is the so called "fork" in the line circuit, converting from 2-wire to 4-wire connection, which causes the leak of speech energy.

Traditionally, delay has been caused by satellite links but today, the digital mobile phones cause a delay because of the speech coding process and the way the speech is transmitted. For that reason, echo cancellers are used on a broader basis in a modern network. The figure below shows the main function of an echo canceller when a digital mobile phone is connected to an analogue telephone in the fixed network.
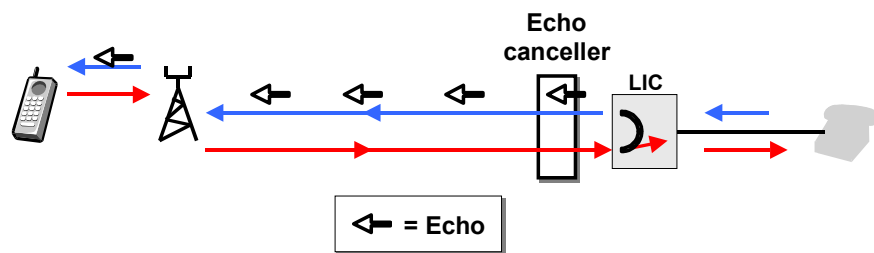

Figure 4- 31 The position and function of an echo canceller

Echo cancellers are also pooled, just as the transcoders, and connected to the speech path if needed. This reduces the total number of echo cancellers and it creates redundancy. Faulty echo cancellers are simply blocked and not connected. The figure below shows the main principle of pooled echo cancellers.
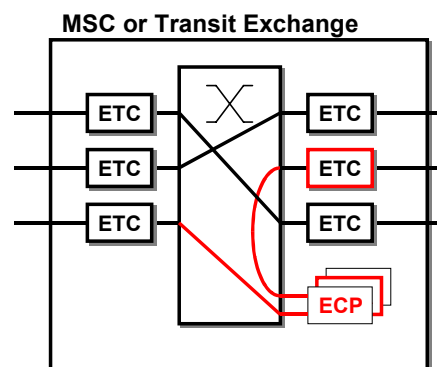

Figure 4- 32 Pooled echo cancellers

THE NEW ECP HARDWARE

Also the echo cancellers are made on the common speech processing platform CSPB, Common Speech Processing Board. The ECP is, just as the transcoder, also located in the new GEM subrack and connected to the group switch via the backplane interface. The capacity has increased significantly as can be seen in the table below.

	ECP 404	ECP5
Channels per board	32	128
Capacity	1	4
Volume	1	1/4
Power consumption	1	1/2

Figure 4- 33 Comparison with previous echo canceller generation

PDSPL-2E

Some abbreviations are longer than others. This is probably one of the longest within Ericsson. The abbreviation PDSPL-2E stands for "second enhanced generation Pooled Digital Signalling Platform Loadable". Easy…

BACKGROUND

In a telephone exchange, there are several types of devices that send tones of various types. Examples are analogue signalling devices and tones sent and received to/from subscribers. In the older versions of AXE, based on BYB 202, each type of tone sending was performed by separate devices. Some years ago, the common hardware PDSPL1 in BYB 202 was developed. Still, there where different boards for different functions.

When BYB 501 was released in 1997, the PDSPL-2H was released at the same time. This was a general hardware platform for tone sending but the boards came pre-programmed from the factory. To add new devices of a specific type, the customer had to order a PDSPL board with the correct identity (index) to get the desired functionality. The board is housed by the GDM subrack and it occupied 40 mm of space.

With the PDSPL-2E, the customer can buy a general board, which is empty when delivered from Ericsson, and then load it with the desired function. The figure below shows the evolution.
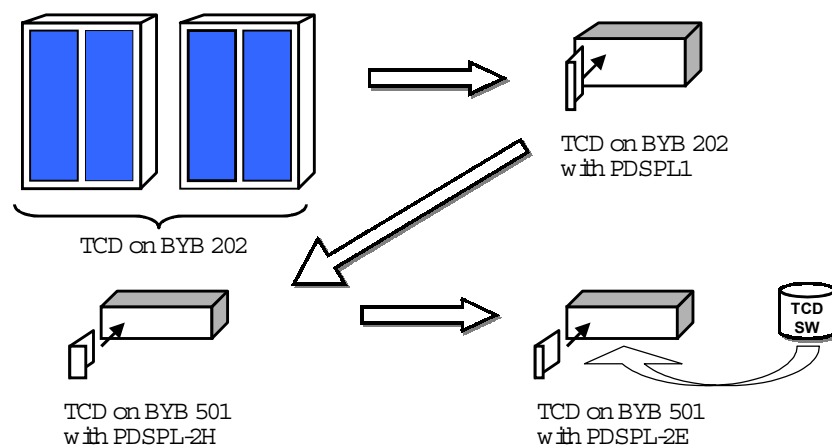

TCD on BYB 202

TCD on BYB 202
with PDSPL1

TCD on BYB 501
with PDSPL-2H

TCD on BYB 501
with PDSPL-2E

TCD SW

Figure 4- 34 Evolution of PDSPL (example of a TCD application)

The functions that are implemented in PDSPL-2E are:

- CSR, Code Sender Receiver
  The device is used for analogue signalling such as MFC,

MFP or CCITT No 5 signalling. The signalling is made with tones. For software compatibility, one board supports 16 CSR devices.

- TCD (Transceiver Check Device) performs trunk line continuity checks.

- CAT (Code Answer and Tone Sender) is a fully programmable sender for all sorts of maintenance tones and sequences. Through the use of commands, it is possible to define any type of tone as well as complete code answers through the linking of tones and idle/zero.

- TRU (Tone Receiving Units) is a tone receiver used by the GTT and PRT AXE functions. GTT (Generated Test Traffic) generates calls to exchanges with code answering equipment. The TRU unit detects and verifies the incoming code answers. GTT is only used in conjunction with A-law. PRT (Progression Test) is a related function that is in employed in markets where μ-law is used.

- KRD (Key-set Code Receiver Device) is used as a DTMF receiver combined with a dial-tone tone sender. KRD is capable of sending either a single tone, a sum of two tones or an amplitude modulated tone with carrier suppression. Both A- and μ-law coding is supported.

- CSKD (Code Sender Key-set Device) is used as a DTMF sender. Both A- and μ-law coding is supported.

- CSFSKD (Code Sender FSK Device, FSK meaning Frequency Shift Keying) is a sender for calling-line identification. Both A- and μ-law coding is supported.

- CCD (Conference Call Device) is the hardware supporting the Multi Junctor Function. Multi Junctor is a platform function that allows the connection of more than two participants to a call. The Multi Junctor Function supports two main functions (monitoring and multi party call) that are independent of one another. Six supplementary functions are associated with these two main functions, i.e., internal connection, speech attenuation, tone sending, speech control, comfort noise and companding law.

GENERAL SYSTEM DESCRIPTION

The common denominator for PDSPL devices is that they are connected to the group switch and in that way "pooled". This means that a group of devices is shared among all subscribers in the exchange. The advantage is that resources are utilised efficiently and that single faults do not stop traffic (you can take another device in the pool of one is blocked). The PDSPL

devices are connected to the group switch via DL2 interfaces going in the backplane of the Generic Device Magazine (GDM). The RP is the link between the PDSPL device and the Central Processor. Please study the figure below.
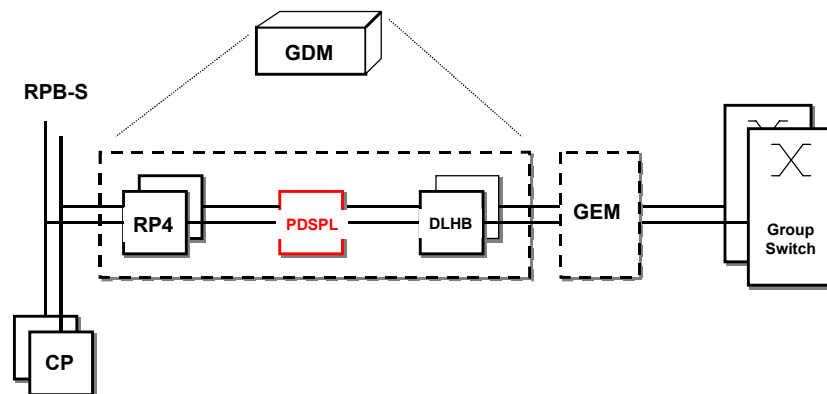

Figure 4- 35 The PDSPL in AXE

The CP has a path to the PDSPL via the RP4 in the GDM subrack. Via the DLHB boards and the GEM subrack, the PDSPL has a path to the group switch. From the group switch, both locally connected subscribers as well as subscribers connected via incoming lines, can be served by any PDSPL within the exchange. Notice that it is not possible to mix old and new PDSPL boards within the same magazine.

HARDWARE

The hardware is build-up around a few main components:

- One device processor with RAM memory.

- One interface circuit which has EM bus interface as well as DL2 interface to the group switch. The circuit is an ASIC as both EMB and DL2 are proprietary interfaces.

- Three Digital Signalling Processors (DSP) which are connected to the DL2 interface as well as internally connected.

- A flash memory for storage of the loaded software. The contents of the flash memory is copied to the RAM memory of the processor as well as to the internal memory of the DSPs when the board is reset.
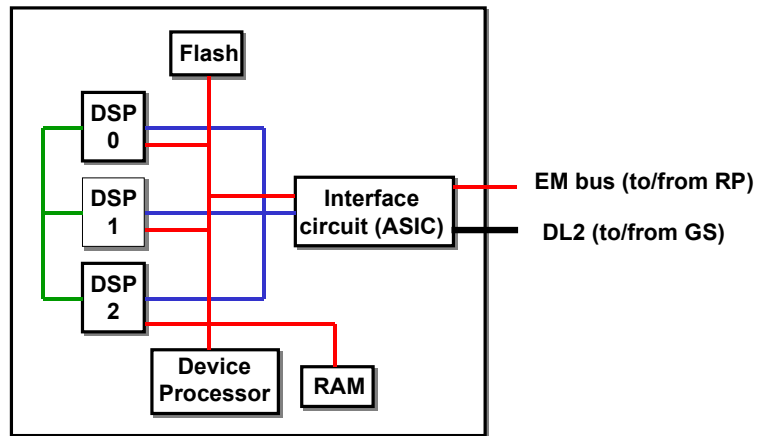
Figure 4- 36 shows the main hardware components.

Figure 4- 36 The hardware of the PDSPL-2E board

The size of the PDSPL circuit board has been reduced to 50% compared with previous version. The functionality of the PDSPL circuit board has not been changed but the size has been reduced. Please study Figure 4- 37 below.
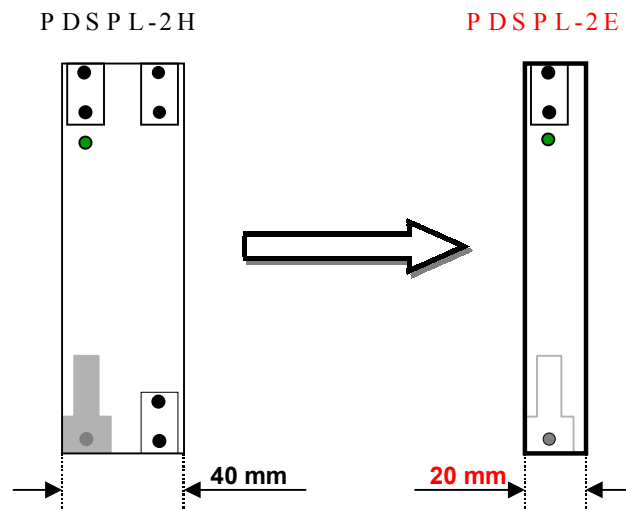

Figure 4- 37 The size has been reduced of the PDSPL circuit board

THE LOAD FUNCTION

When the PDSPL boards leave the factory, they are "empty". This means that no function is tied to the hardware and the flash memory is empty.

To load the firmware on the PDSPL boards, two things are needed:

- The PDSPL Application Loader (PDAL) function. This function makes it possible to load the PDSPL boards with firmware stored in the CP.

- The APZ 10.0 operating system or higher

It is not possible to mix loadable and not loadable PDSPL boards in the same subrack. In the exchange, it is possible to have a mix between the "old" and the new PDSPL hardware.

The PDSPL hardware can be mixed with any other type of hardware adapted for the GDM subrack. The only limit is the capacity of the RP.

The loading of firmware start by loading them into the Program Store (PS) of the central processor. The loading is done from the IOG/APG. Two software units handle the loading; one in the central processor and one in the regional processor. Please study the figure below.
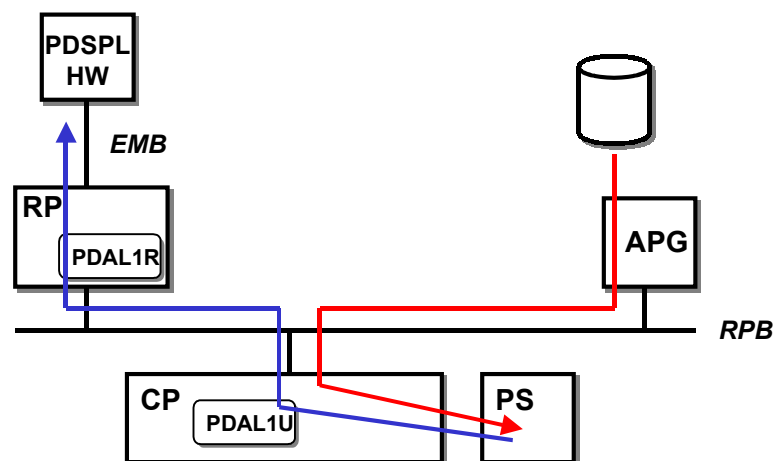

Figure 4- 38 Overview of the firmware loading using PDAL

The function also has two tables:

- A licence and configuration table
  The table stores information about which of the applications that are free to use. This makes it possible for Ericsson to licence functions to operators. When the licence fee is paid, the application can be used by the operator in as many PDSPL boards as they wish.

- A downloaded EM table
  The table stores information about firmware that has been loaded in PDSPL boards. The table is updated after successful loading of firmware.

The downloading and configuring of the function is using the standard AXE commands for definition of EMs. EXEMI is used

to define the function of the board and the actual download of firmware takes place after the `BLEME` command. Loading of firmware into the PS is done with `LAEUL`.

ATM LINK INTERFACE, ALI

ATM will be used extensively in the 3:rd generation mobile system as bearer of voice and data. In the case of AXE, ATM will be used in cases where ATM is used to access the radio part of UMTS (referred to as UTRAN). Different scenarios are defined to how the future network will evolve and the figure below shows one possible scenario where an existing GSM operator adds an UTRAN network and lets his existing AXE switches interface to this network. This means that AXE needs and ATM interface that can handle voice, data and SS7 signalling.
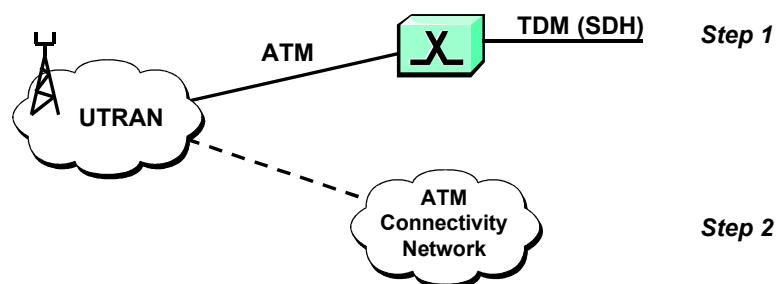

Figure 4- 39 AXE interfaces the ATM network in UTRAN

The interface is an optical 155 Mbit/s interface that supports different ATM services. Voice and data will use AAL2 while signalling uses AAL5. In the case of signalling, the ALI will include signalling parts which enables it to extract the signalling and send it to the CP for analysis. Please study the example in the figure below.
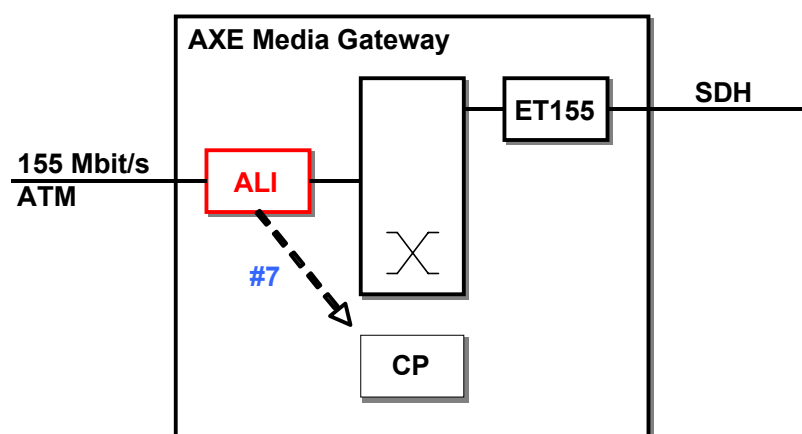

Figure 4- 40 Signalling on AAL5

The UTRAN network uses another format on the speech than the "standard" PCM format used in the fixed network. For that reason, a transcoder has to be included in the call to change the format to PCM (64 kbit/s). The system uses an internal HDLC-

based format between the ALI and the Transcoder (TRA). AAL2 is used and the ALI can in the first release handle 480 channels. Permanent Virtual Circuits (PVC) are set-up between the ALI and different end points and AAL2 signalling can be used inside these PVCs to establish and release calls (Q.AAL2 signalling). Please study the figure below.
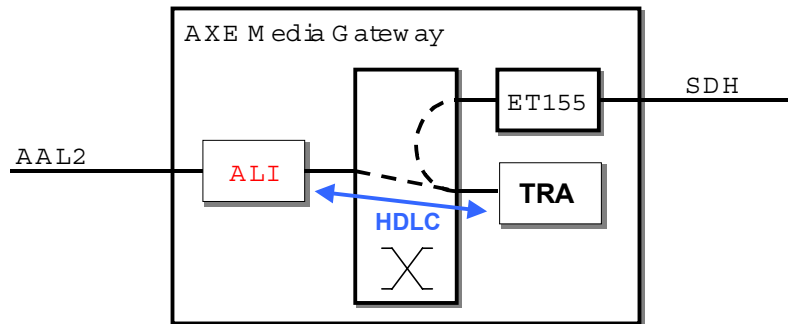

Figure 4- 41 The ALI is used for coded AAL2 transmission

The ALI can also handle 64 kbit/s speech on AAL2. In that cane, no TRA is need to change the coding of the speech (it is done in the UTRAN network). The ALI can in the first release handle 480 channels.

In case of circuit switched data, ATM will carry data in cells which will terminate in a so called Data Transmission Interface (DTI). This equipment is in GSM referred to as Interworking Unit (IWU). The ALI can handle 8 channels of circuit switched data. Note: 8 channels does not seem to be enough but consider that most of the data traffic in 3:rd generation mobile system will go over packet switched networks built on IP or ATM. The figure below gives an example of an ALI handling circuit switched data as well as 64 kbit/s un-coded speech.
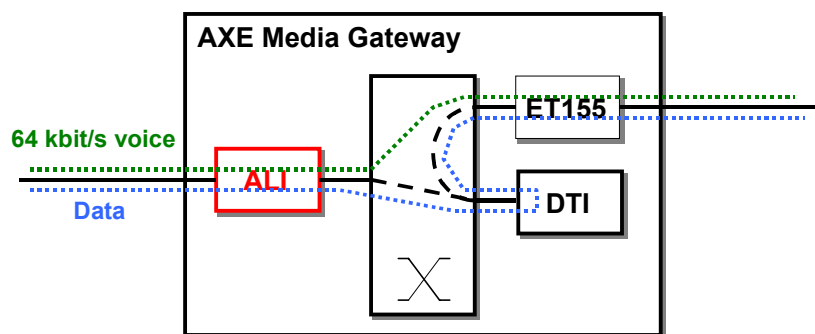

Figure 4- 42 The ALI handling both data and 64 kbit/s speech

SIGNALLING LINKS

All types of signalling links are based on the RPP and the RPG platforms. Both these processor types have been described in the APZ chapter (chapter 3) regarding performance and structure. These two following chapters will describe the protocols supported by the APT software.

SS7 SIGNALLING LINKS

All signalling links are based on the RPG3 hardware which is an improvement of the RPG2 regarding capacity. The following signalling standards are supported by the AXE 810 software.

- ITU-T C7, 64 kbit/s
  The signalling terminal fulfils ITU-T Q.703 white book recommendation. One RPG3 can handle 4 signalling links for all traffic mixes.

- ANSI SS7, 64 kbit/s
  The signalling terminal fulfils Bellcore GR-246-CORE. One RPG3 can handle 4 signalling links for all traffic mixes.

- ANSI SS7, 56 kbit/s
  The signalling terminal fulfils Bellcore GR-246-CORE. One RPG3 can handle 4 signalling links for all traffic mixes.

All three signalling terminals are placed in a GDM-H subrack which can have up to 8 RPG3s. This means that one subrack can have up to 32 signalling terminals operating at 64 or 56 kbit/s.

There are also non-GS connected signalling terminals on another platform than RPG. The signalling terminals are placed in GDM2-H subracks with the possibility to have 4 signalling terminals. The three standards supported are:

- ANSI DS0A SS7, 56 kbit/s
  The signalling terminal fulfils Bellcore GR-246-CORE and DS0A maintenance functionality in accordance with Bellcore GR-OPT-000489.

- ANSI V35 SS7, 56 kbit/s
  The signalling terminal fulfils Bellcore GR-246-CORE.

- Japanese J7X21 J7, 48 kbit/s
  The signalling terminal is compliant with Japanese TTC JT-Q.703 and it is programmable to operate in either 4.8 kbit/s or 48 kbit/s.

HIGH-SPEED SIGNALLING LINKS (HSL)

A high-speed link is used in some applications where there is high load on the signalling links. Examples are to Home Location registers (HLR) in mobile networks or to Service Control Points (SCP) for intelligent network services.

An HSL is based on a full 2 Mbit/s (or 1.5 in Japan or the US) used for signalling and the link is terminated in the RPP. This means that a HSL roughly has 30 times the capacity of an ordinary 64/56 kbit/s signalling link. The signalling is based on ATM and the ATM cells are mapped to a standard 2/1.5 Mbit/s ETC or to a tributary of and STM-1 (ET155). Please study the figure below.
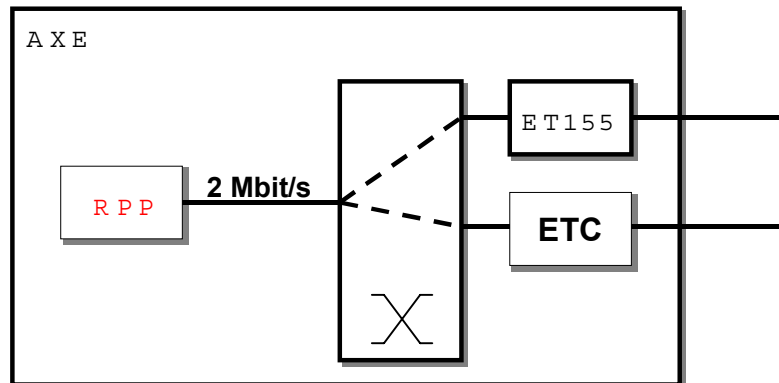

Figure 4- 43 High-speed link for signalling

Two types of HSL standards are supported:

- HSL ETSI, 2048 kbit/s
  One RPP supports one high-speed signalling link for all traffic mixes. The software supports ITU-T Q2110, 2140 and 2144. That corresponds to SSCOP, SSCF and SAAL Layer Management respectively.

- Japanese HSL, 1544 kbit/s
  One RPP supports one high-speed signalling link for all traffic mixes.

Intentionally Blank